IN THE CLAIMS:

All pending claims are set forth below. Cancelled and withdrawn claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (previously amended), (cancelled), (withdrawn), (new), (previously added), (reinstated - formerly claim #), (previously reinstated), (re-presented - formerly dependent claim #), or (previously re-presented).

Please CANCEL claims 16, 20, 21, 25-27, 31-33 and 45 without prejudice or disclaimer. Please AMEND claims 17-19, 22, 24, 28, 30, 34, 36 and 46-48 in accordance with the following:

Sub E1 E1 cont

1. (**previously amended**) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process a pulse stream of data from a DVD or a CD, comprising:

a PLL (Phase Locked Loop) to receive the pulse stream, to generate a PLL clock;

a frame/ID (identification) synchronization detector to latch the pulse stream according to said PLL clock, to generate a symbol clock;

a single demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data;

a memory to store the demodulated data from said demodulator;

an ECC (error checking and correction) decoder to error-correct the demodulated data stored in said memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes, to generate error corrected data;

a descrambler to descramble the error corrected data stored in said memory, in the DVD mode; and

a CD audio processor to process the error corrected data stored in said memory, in the CD mode.

2. (**previously amended**) The combined DVD/CD data processor as claimed in claim 1, wherein the predetermined code length and error correction range in the DVD mode are PI(182,172), PO(208,192), and the predetermined code length and error correction range in the CD mode are C1(32,28), C2(28,24).

3. (**previously amended**) The combined DVD/CD data processor as claimed in claim 2, wherein said ECC decoder comprises:

a syndrome generator to receive said demodulated data from said memory to generate a syndrome polynomial according to said code length and correction range of PI(182,172), PO(208,192) in the DVD mode, and of C1(32,28), C2(28,24) in the CD mode;

an erasure constant generator to receive an erasure flag to generate an erasure constant;

a modified syndrome calculator to receive the syndrome polynomial and the erasure constant to calculate a modified syndrome and generate a Forney syndrome polynomial and an erasure polynomial;

a modified Euclidean algorithm to process the Forney syndrome polynomial and the erasure polynomial based on a modified Euclidean algorithm, to generate an errata locator polynomial and an errata evaluator polynomial; and

a Chien search and error correction circuit to correct errors of the demodulated data stored in said memory according to said errata locator polynomial and said errata evaluator polynomial.

4. (**original**) The combined DVD/CD data processor as claimed in claim 1, wherein said memory is an external memory.

5. (**original**) The combined DVD/CD processor as claimed in claim 1, wherein said memory has a first memory map including a plurality of blocks of the error corrected data each having a first fixed number of bytes in the DVD mode, and a second memory map including a plurality of frames of the error corrected data each having a second fixed number of bytes in the CD mode.

6. (**original**) The combined DVD/CD processor as claimed in claim 5, wherein:

the plurality of blocks is 13;

the first fixed number of bytes is 32.25 Kbytes;

the plurality of frames is 256; and

the second fixed number of bytes is 32 bytes.

7. (**previously amended**) A combined DVD (Digital Video Disk)/CD (Compact Disk)

data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks;

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

a single demodulator to perform a first type of demodulation on the first pulse stream according to the first symbol clock to generate first demodulated data of a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate second demodulated data of a CD mode;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range and to store the error corrected first demodulated data back in said memory, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range and to store the error corrected second demodulated data back in said memory.

8. (**original**) The combined DVD/CD data processor as claimed in claim 7, wherein said memory comprises:

a first memory map to store the error corrected second demodulated data; and

a second memory map different from the first memory map, to store the error corrected second demodulated data.

9. (**original**) The combined DVD/CD data processor as claimed in claim 8, wherein said first memory map provides a VBR (variable bit rate) control margin to interface the error corrected first demodulated data with an audio/video decoder.

10. (**previously amended**) The combined DVD/CD data processor as claimed in claim 7, wherein said ECC decoder comprises:

a syndrome generator to generate syndrome polynomials from the first and second demodulated data stored in said memory in accordance with the corresponding first and second

code lengths and corresponding first and second correction ranges;

an erasure constant generator to generate first and second erasure constants from corresponding first and second erasure flags;

a modified syndrome calculator to generate first and second Forney syndrome polynomials and first and second erasure polynomials from the corresponding first and second erasure constants and the corresponding syndrome polynomials;

a modified Euclidean algorithm to process the first and second Forney syndrome polynomials with the corresponding first and second erasure polynomials, to generate corresponding first and second errata locator polynomials and corresponding first and second errata evaluator polynomials; and

a Chien search and error correction unit to correct errors of the first and second demodulated data stored in said memory according to the corresponding first and second errata locator polynomials and the corresponding first and second errata evaluator polynomials.

11. (**original**) The combined DVD/CD data processor as claimed in claim 7, further comprising:

a descrambler to descramble the error corrected first demodulated data stored in said memory for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data stored in said memory.

12. (**previously amended**) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a single demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range in the DVD mode, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range in the CD mode.

13. (**previously amended**) The combined DVD/CD data processor as claimed in claim 12, wherein said memory stores the error corrected first demodulated data output from said ECC decoder in a first memory map, and the error corrected second demodulated data output from said ECC decoder in a second memory map different from the first memory map.

14. (**original**) The combined DVD/CD data processor as claimed in claim 12, further comprising:

a descrambler to descramble the error corrected first demodulated data stored in said memory for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data stored in said memory.

15. (**original**) The combined DVD/CD data processor as claimed in claim 12, further comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks; and

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

wherein said demodulator performs a first type of demodulation on the first pulse stream according to the first symbol clock to generate the first demodulated data in the DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate the second demodulated data in the CD mode.

16. (**cancelled**)

17. (**currently amended**) ~~The combined DVD/CD as claimed in claim 16,~~ A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

a single external memory to store the first and second demodulated data; and

a single ECC (error checking and correction) decoder to error correct the first and

second demodulated data stored in said memory, wherein said single ECC decoder error corrects the first and second demodulated data stored in said memory in accordance with corresponding different code lengths and correction ranges.

18. (**currently amended**) The combined DVD/CD data processor as claimed in claim ~~16~~ 17, further comprising:

a descrambler to descramble the error corrected first demodulated data for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data.

19. (**currently amended**) The combined DVD/CD data processor as claimed in claim ~~16~~ 17, further comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks; and

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

wherein said demodulator performs a first type of demodulation on the first pulse stream according to the first symbol clock to generate the first demodulated data in a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate the second demodulated data in a CD mode.

20. (**cancelled**)

21. (**cancelled**)

22. (**currently amended**) ~~The data processor apparatus as claimed in claim 20,~~ A data processor apparatus for common use in a DVD (Digital Video Disk)/CD (Compact Disk) player using discrimination information provided according to a DVD or a CD, comprising:

a single pre-processor generating a clock from a pulse stream read from one of the DVD and the CD and performing demodulation of the pulse stream according to the discrimination information and the generated clock;

a memory unit storing the demodulated pulse stream processed by the single pre-

processor as data in a corresponding format according to the discrimination information; and

a data processor and converter processing the data stored in the memory unit;

wherein:

the data processor and converter comprises an error corrector error-correcting the data stored in the memory unit according to the discrimination information using a preset error correcting method; and

the data processor and converter audio-converts or data-converts the processed data according to the discrimination information.

23. (**previously added**) The data processor apparatus as claimed in claim 22, wherein the preset error correcting method of the error corrector depends on a code length and a correcting range according to the discrimination information.

24. (**currently amended**) The data processor apparatus as claimed in claim ~~20~~ 22, wherein the memory unit comprises:

a data storage memory; and

a memory controller controlling the memory to store the data in the corresponding format according to the discrimination information.

25. (**cancelled**)

26. (**cancelled**)

27. (**cancelled**)

28. (**currently amended**) ~~The data processor apparatus as claimed in claim 25,~~ A data processor apparatus for sharing a memory according to discrimination information which depends on a type of an information storage medium which stores data, comprising:

a single pre-processor performing demodulation of the data according to the discrimination information;

a memory unit storing the demodulated data processed by the single pre-processor in a corresponding format according to the discrimination information; and

a data processor and converter processing the data stored in the memory unit;

wherein:

the single pre-processor generates a clock from a pulse stream read from the information storage medium;

the data processor and converter audio-converts or data-converts the processed data according to the discrimination information; and

the data processor and converter comprises an error corrector error-correcting the data stored in the memory unit according to the discrimination information using a preset error correcting method.

29. (**previously added**) The data processor apparatus as claimed in claims 28, wherein the preset error correcting method of the error corrector depends on a code length and a correcting range according to the discrimination information.

30. (**currently amended**) The data processor apparatus as claimed in claim ~~25~~ 28, wherein the memory unit comprises:

a data storage memory; and

a memory controller controlling the memory to store the data in the corresponding format according to the discrimination information.

31. (**cancelled**)

32. (**cancelled**)

33. (**cancelled**)

34. (**currently amended**) ~~The optical disk drive as claimed in claim 31,~~ An optical disk drive, comprising:

a controller determining a type of a disk through a signal read from the disk and outputting discrimination information according to the disk type;

a single pre-processor performing demodulation of data from the disk according to the discrimination information;

a memory unit storing the demodulated data processed by the single pre-processor in a corresponding format according to the discrimination information; and

a data processor and converter processing the data stored in the memory unit;

wherein:

the single pre-processor generates a clock from a pulse stream read from the disk;

the data processor and converter audio-converts or data-converts the processed data according to the discrimination information, and

the data processor and converter comprises an error corrector error-correcting the data stored in the memory unit according to the discrimination information using a preset error correcting method.

35. (**previously added**) The optical disk drive as claimed in claim 34, wherein the preset error correcting method of the error corrector depends on a code length and a correcting range according to the discrimination information.

36. (**currently amended**) The optical disk drive as claimed in claim ~~31~~ 34, wherein the memory unit comprises:

a data storage memory; and

a memory controller controlling the memory to store the data in the corresponding format according to the discrimination information.

37. (**previously added**) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process a pulse stream of data from a DVD or a CD, comprising:

a PLL (Phase Locked Loop) to receive the pulse stream, to generate a PLL clock;

a frame/ID (identification) synchronization detector to latch the pulse stream according to said PLL clock, to generate a symbol clock;

a demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data;

a memory to store the demodulated data from said demodulator;

an ECC (error checking and correction) decoder to error-correct the demodulated data stored in said memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes, to generate error corrected data, wherein the predetermined code length and error

correction range in the DVD mode are PI(182,172), PO(208,192), and the predetermined code length and error correction range in the CD mode are C1(32,28), C2(28,24);

a descrambler to descramble the error corrected data stored in said memory, in the DVD mode; and

a CD audio processor to process the error corrected data stored in said memory, in the CD mode.

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38. (**previously added**) The combined DVD/CD data processor as claimed in claim 37, wherein said ECC decoder comprises:

E1 Cont

a syndrome generator to receive said demodulated data from said memory to generate a syndrome polynomial according to said code length and correction range of PI(182,172), PO(208,192) in the DVD mode, and of C1(32,28), C2(28,24) in the CD mode;

an erasure constant generator to receive an erasure flag to generate an erasure constant;

a modified syndrome calculator to receive the syndrome polynomial and the erasure constant to calculate a modified syndrome and generate a Forney syndrome polynomial and an erasure polynomial;

a modified Euclidean algorithm to process the Forney syndrome polynomial and the erasure polynomial based on a modified Euclidean algorithm, to generate an errata locator polynomial and an errata evaluator polynomial; and

a Chien search and error correction circuit to correct errors of the demodulated data stored in said memory according to said errata locator polynomial and said errata evaluator polynomial.

39. (**previously added**) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process a pulse stream of data from a DVD or a CD, comprising:

a PLL (Phase Locked Loop) to receive the pulse stream, to generate a PLL clock;

a frame/ID (identification) synchronization detector to latch the pulse stream according to said PLL clock, to generate a symbol clock;

a demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data;

a memory to store the demodulated data from said demodulator;

an ECC (error checking and correction) decoder to error-correct the demodulated data stored in said memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes, to generate error corrected data;

a descrambler to descramble the error corrected data stored in said memory, in the DVD mode; and

a CD audio processor to process the error corrected data stored in said memory, in the CD mode,

wherein said memory has a first memory map including a plurality of blocks of the error corrected data each having a first fixed number of bytes in the DVD mode, and a second memory map including a plurality of frames of the error corrected data each having a second fixed number of bytes in the CD mode.

40. (**previously added**) The combined DVD/CD processor as claimed in claim 39, wherein:

the plurality of blocks is 13;

the first fixed number of bytes is 32.25 Kbytes;

the plurality of frames is 256; and

the second fixed number of bytes is 32 bytes.

41. (**previously added**) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks;

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

a demodulator to perform a first type of demodulation on the first pulse stream according to the first symbol clock to generate first demodulated data of a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate second demodulated data of a CD mode;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range and to store the error corrected first demodulated data back in said memory, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range and to store the error corrected second demodulated data back in said memory, wherein said memory comprises:

a first memory map to store the error corrected second demodulated data; and

a second memory map different from the first memory map, to store the error corrected second demodulated data.

E1 cont

42. (**previously added**) The combined DVD/CD data processor as claimed in claim 41, wherein said first memory map provides a VBR (variable bit rate) control margin to interface the error corrected first demodulated data with an audio/video decoder.

F1 cont

43. (**previously added**) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks;

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

a demodulator to perform a first type of demodulation on the first pulse stream according to the first symbol clock to generate first demodulated data of a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate second demodulated data of a CD mode;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range and to store the error corrected first demodulated data back in said memory, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range and to store the error corrected second demodulated data back in said memory,

wherein said ECC decoder comprises:

a syndrome generator to generate syndrome polynomials from the first and second demodulated data stored in said memory in accordance with the corresponding first and second code lengths and corresponding first and second correction ranges,

an erasure constant generator to generate first and second erasure constants from corresponding first and second erasure flags,

E1 cont

a modified syndrome calculator to generate first and second Forney syndrome polynomials and first and second erasure polynomials from the corresponding first and second erasure constants and the corresponding syndrome polynomials,

E1 Cont

a modified Euclidean algorithm to process the first and second Forney syndrome polynomials with the corresponding first and second erasure polynomials, to generate corresponding first and second errata locator polynomials and corresponding first and second errata evaluator polynomials, and

a Chien search and error correction unit to correct errors of the first and second demodulated data stored in said memory according to the corresponding first and second errata locator polynomials and the corresponding first and second errata evaluator polynomials.

44. (**previously added**) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range in the DVD mode, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range in the CD mode,

wherein said memory stores the error corrected first demodulated data output from said ECC decoder in a first memory map, and the error corrected second demodulated data output from said ECC decoder in a second memory map different from the first memory map.

45. (**cancelled**)

46. (**currently amended**) ~~The combined DVD/CD as claimed in claim 45,~~ A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a single demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

an external memory to store the first and second demodulated data; and

a single ECC (error checking and correction) decoder to error correct the first and second demodulated data stored in said memory;

wherein said single ECC decoder error corrects the first and second demodulated data stored in said memory in accordance with corresponding different code lengths and correction ranges.

47. (**currently amended**) The combined DVD/CD data processor as claimed in claim ~~45~~ 46, further comprising:

a descrambler to descramble the error corrected first demodulated data for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data.

48. (**currently amended**) ~~The combined DVD/CD data processor as claimed in claim 45, further comprising:~~ A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a single demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

an external memory to store the first and second demodulated data;

a single ECC (error checking and correction) decoder to error correct the first and second demodulated data stored in said memory;

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks; and

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

wherein said demodulator performs a first type of demodulation on the first pulse stream according to the first symbol clock to generate the first demodulated data in a DVD mode, and a

second type of demodulation on the second pulse stream according to the second symbol clock to generate the second demodulated data in a CD mode.